Platform and Research overview on the Intel Single-chip Cloud Computer

Invited talk at EPITA, Paris

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Informatics Institute
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October 17, 2012

Outline

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About me

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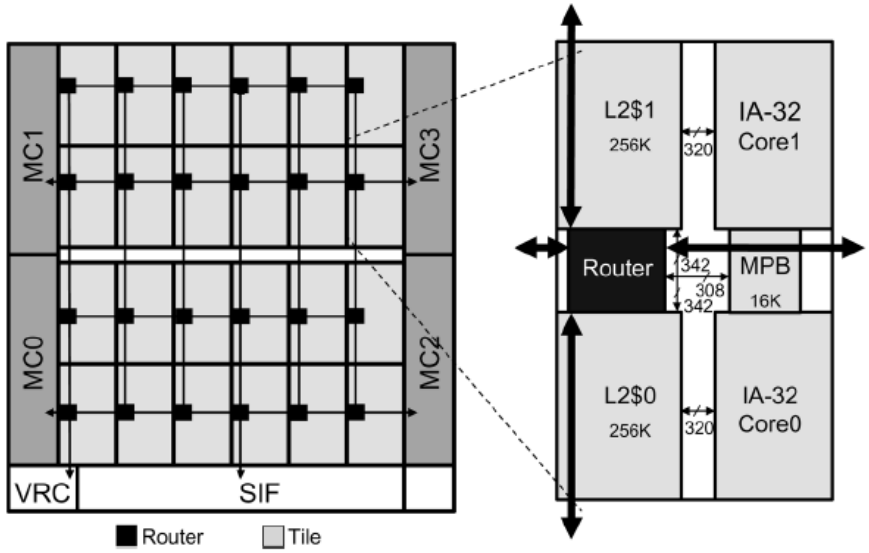
- Experimental research platform
- 6×4 Mesh network (24 tiles).
- 2 Cores per tile (48 total).



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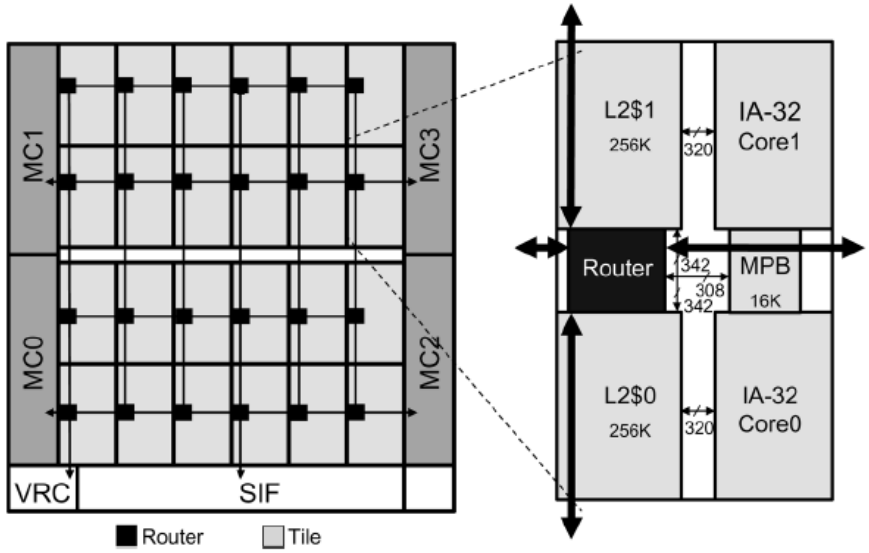

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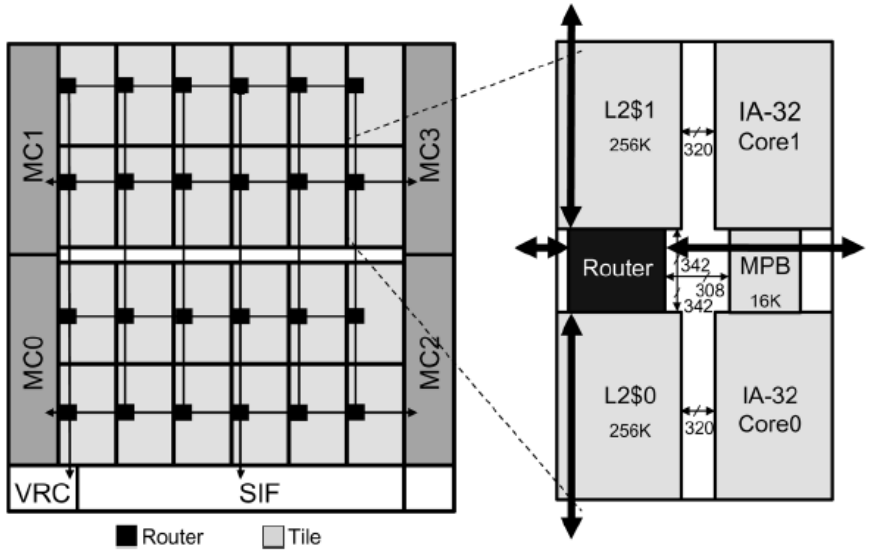

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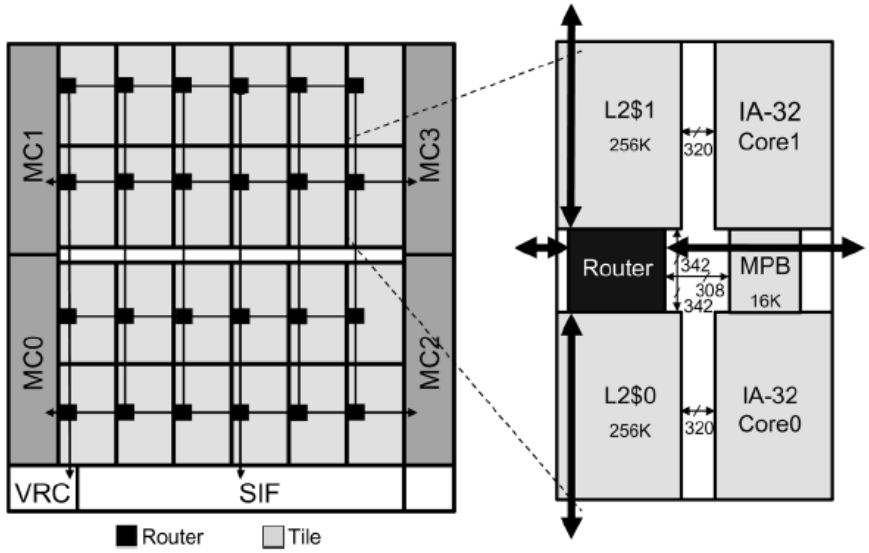

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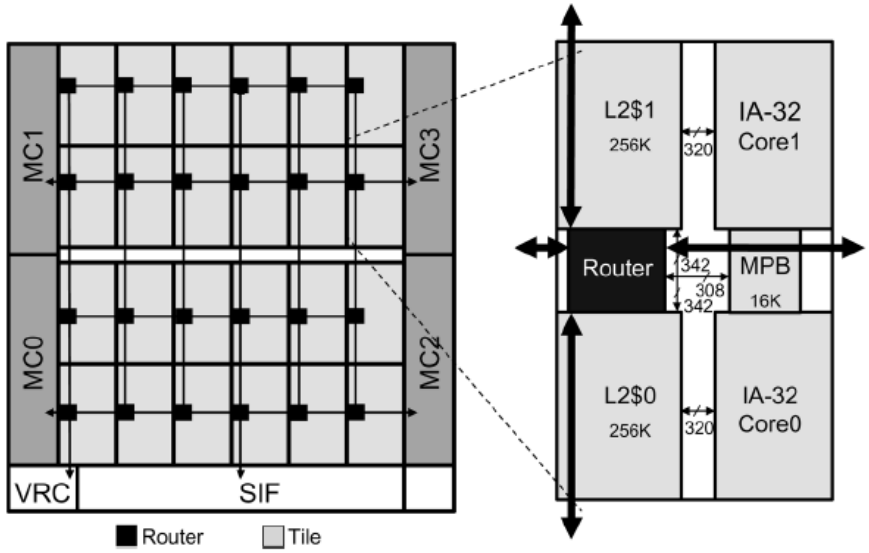
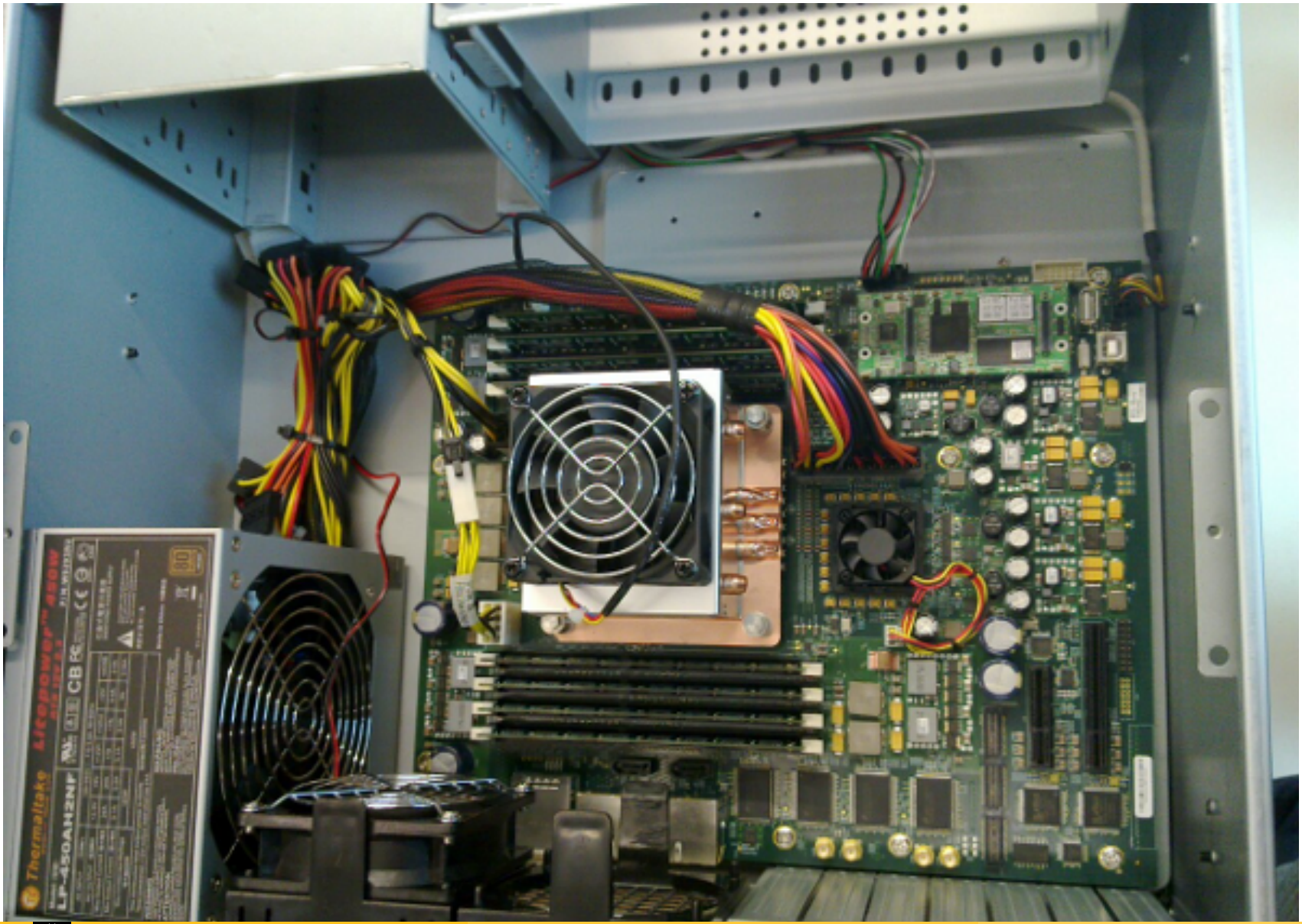
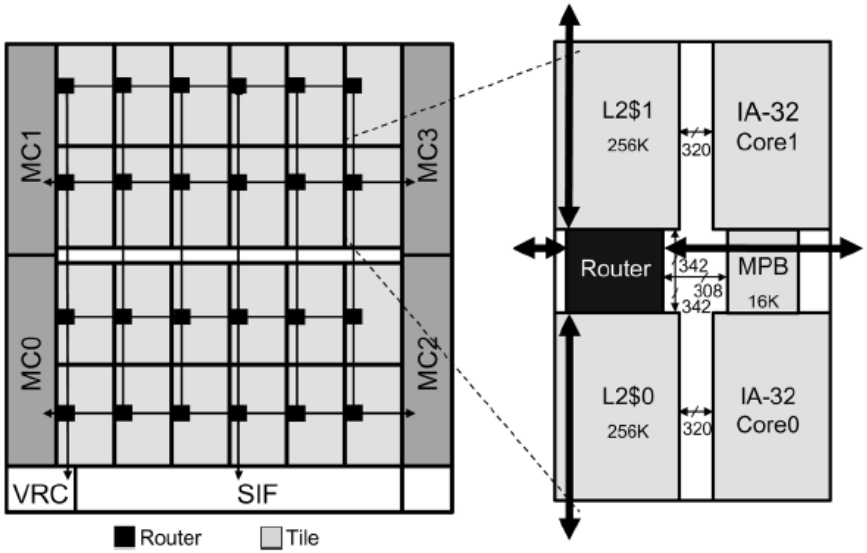
- Control through FPGA and PCIe / Ethernet to MCPC (Linux Box)



The Hardware



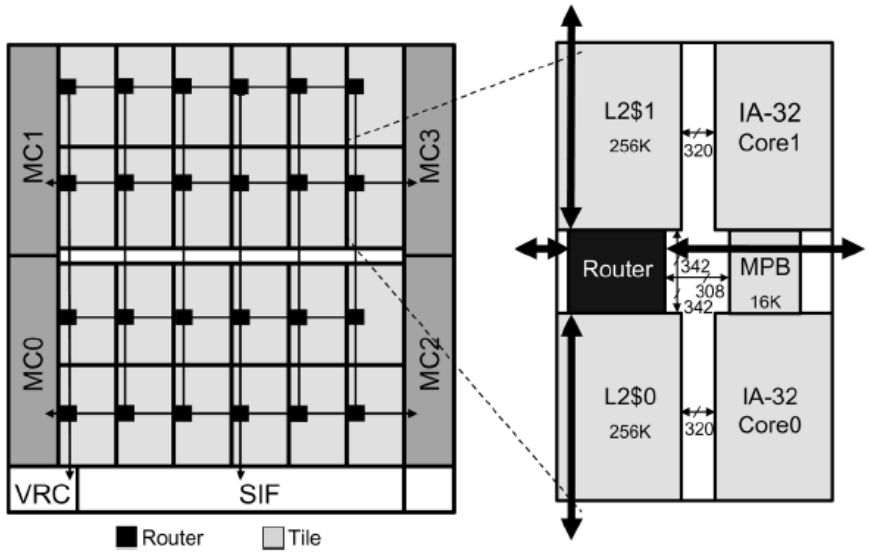
Network Layout



- Mesh network (6×4)
- 800-1600MHz
- 2Tb/s bisection bandwidth
- XY routing protocol
- 5 mesh cycles per hop (4-stage router)

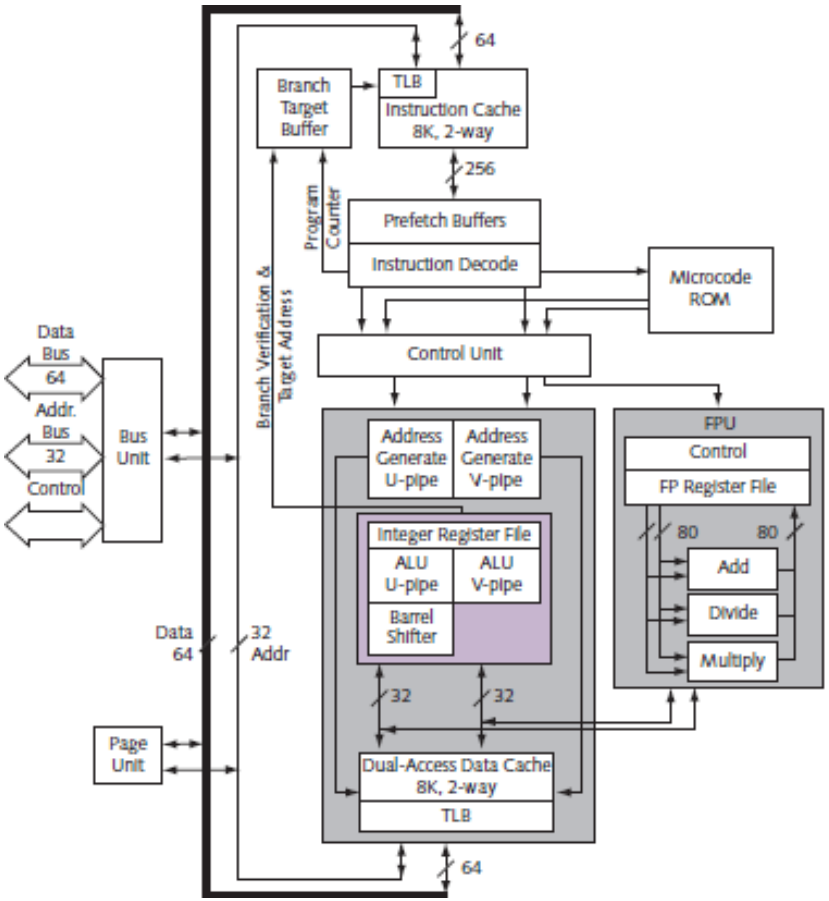
Tile Layout

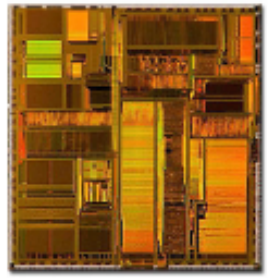
- Five port crossbar router.
- Two P54C (Pentium 1) cores.
- L1 instruction cache and L1 data cache (both 16KB) per core.
- 256KB L2 cache per core.
- 16KB shared on-chip memory (*Message Passing Buffer*).
- Configuration register bank.

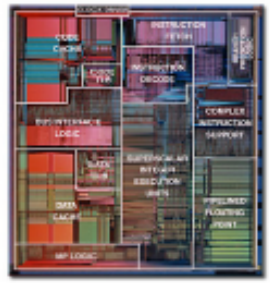


Core

- P54C (1994)
- 100MHz original, for SCC 100MHz-1GHz
- 3.3V original, for SCC 0.7V-1.14V
- Superscalar (dual integer pipe)
- in-order execution
- Only allows single outstanding memory operation

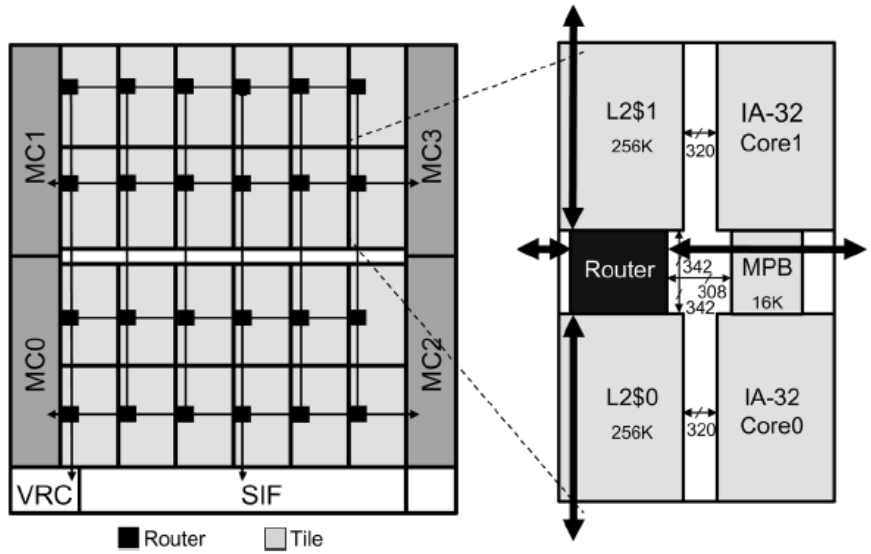






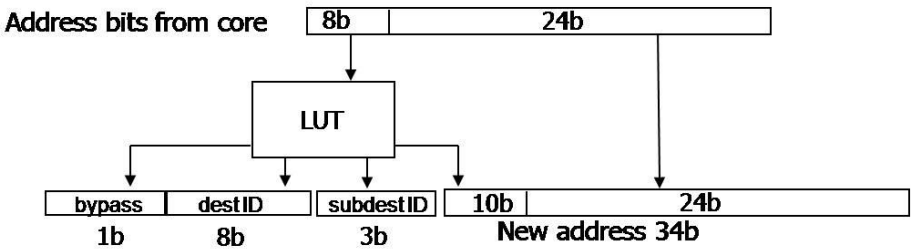
Memory System

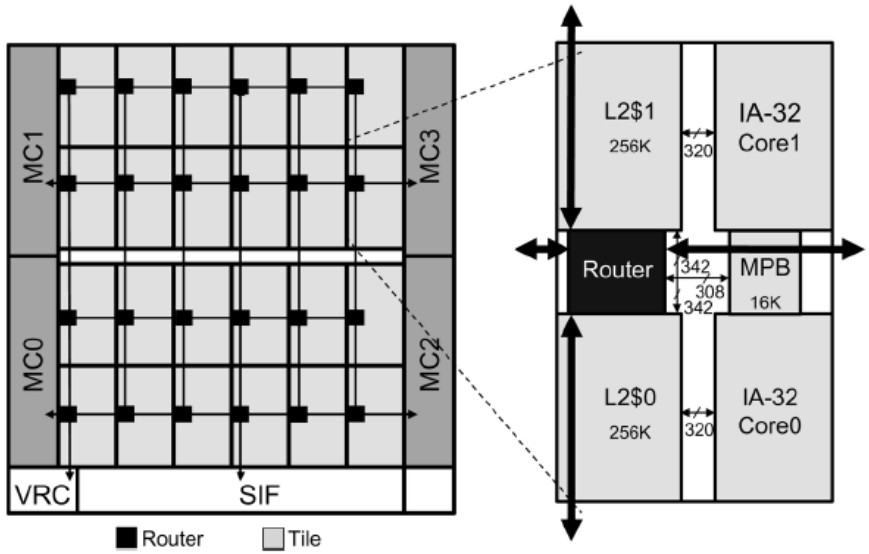
- 4 Memory Controllers, 8 GB per controller (32GB total).
- 32 bit address space for the cores (4GB Max).



Memory System

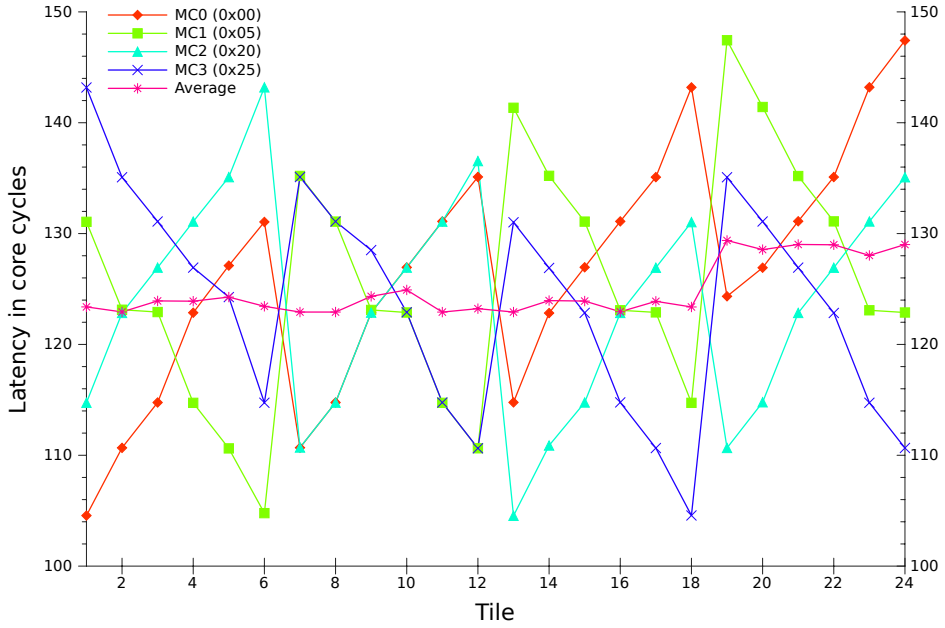
- 4 Memory Controllers, 8 GB per controller (32GB total).
- 32 bit address space for the cores (4GB Max).
- Lookup tables map core addresses to physical addresses with routing information.
- Resulting in 256 $\times$ 16MB *LUT pages*.
- LUT mapping can be changed at runtime, by all cores.

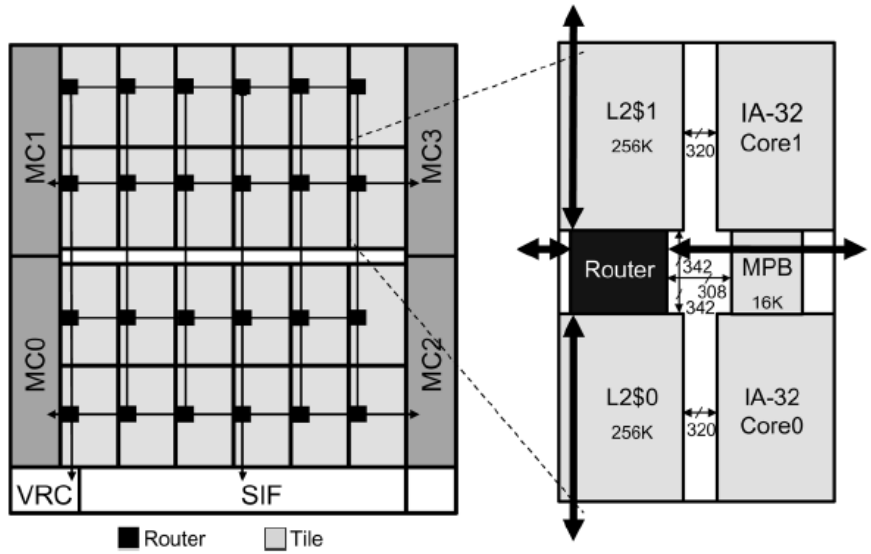




Memory: Latency Differences

- Latency and throughput are depending on the distance to the memory controller.
- Average about the same except for upper row of tiles.





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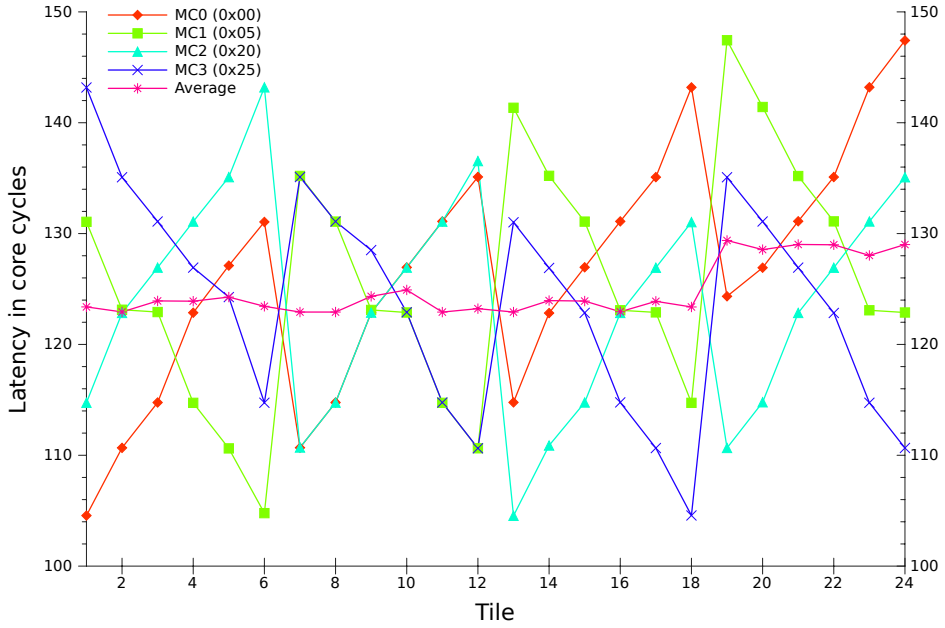

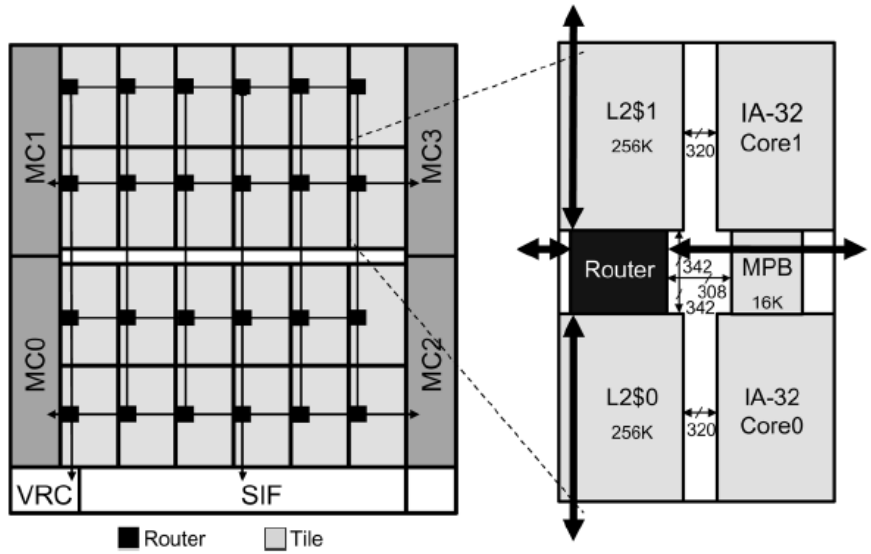

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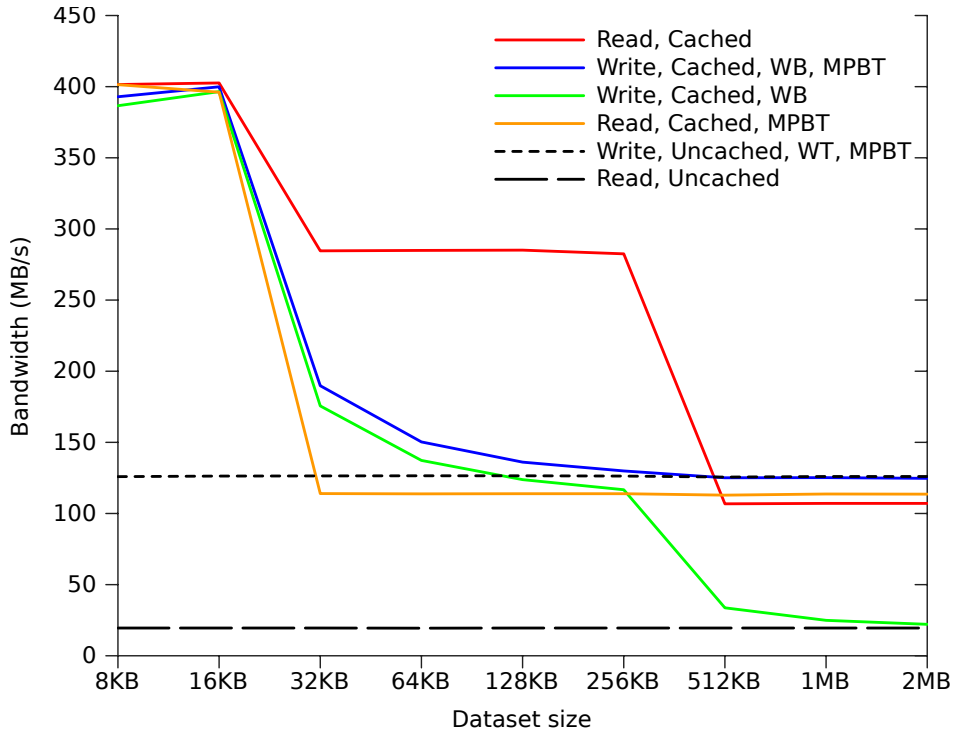

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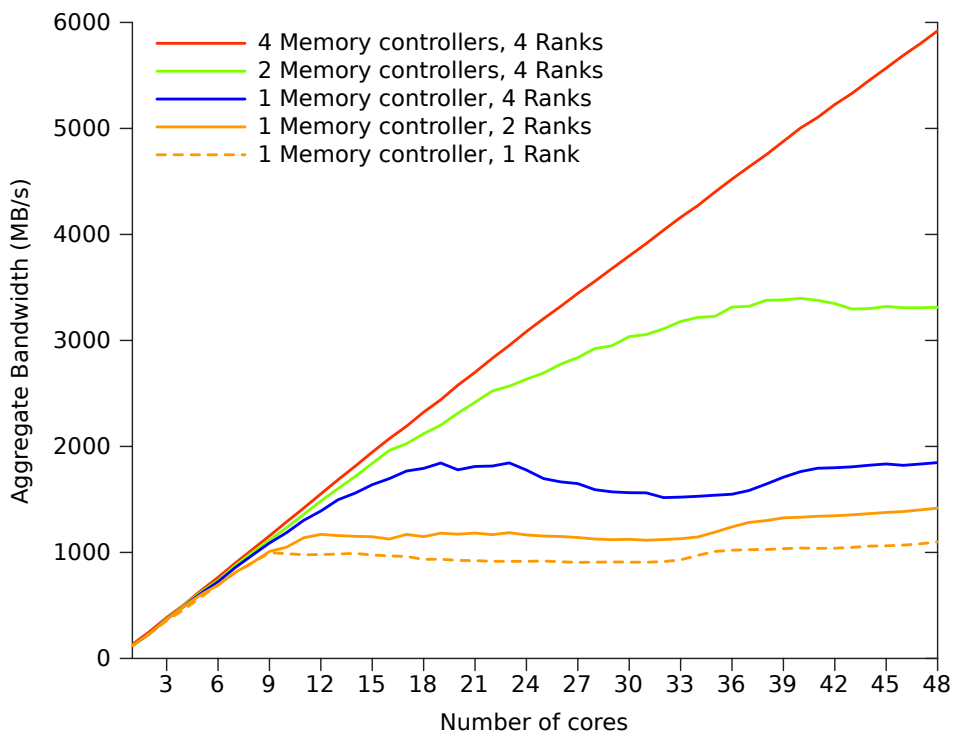

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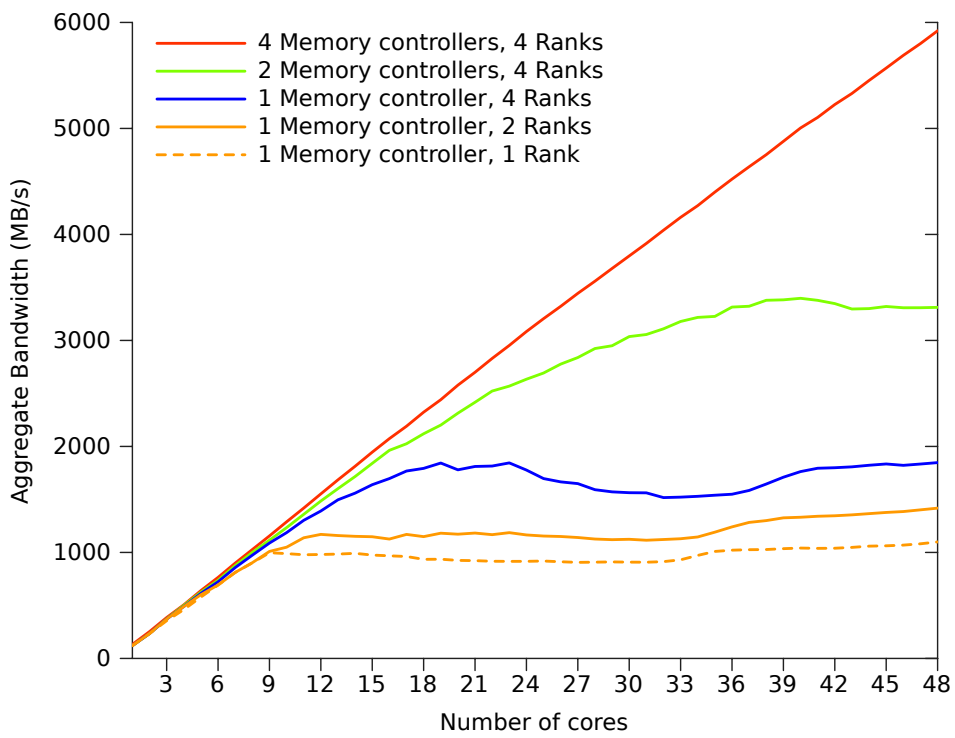

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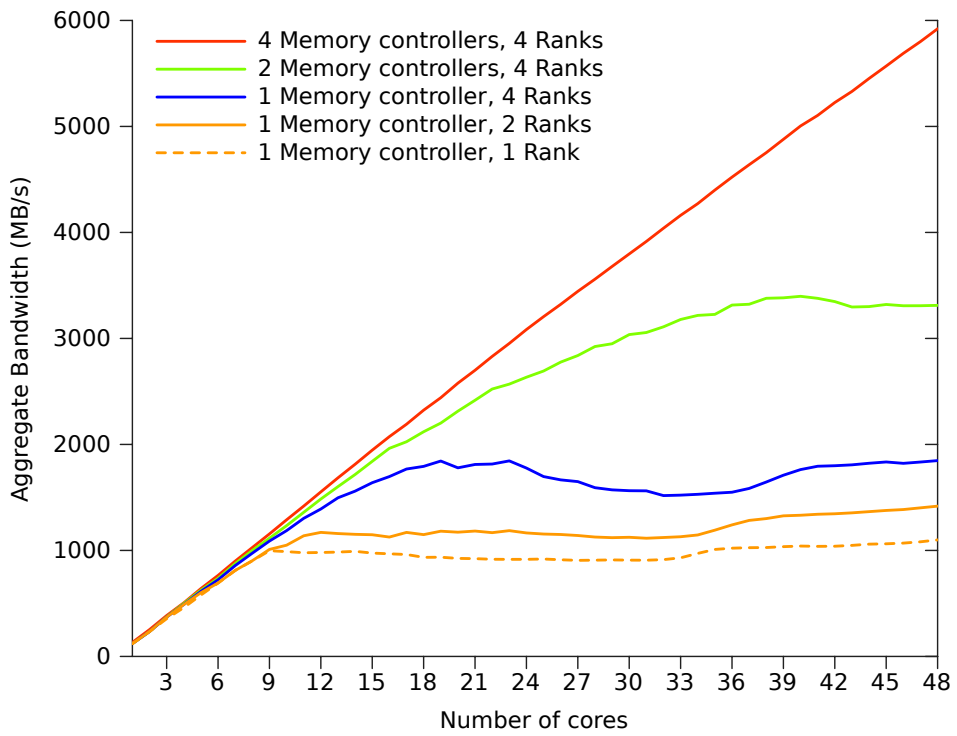
- Large memory copy operations can be performed in parallel by multiple *Copy Cores*.



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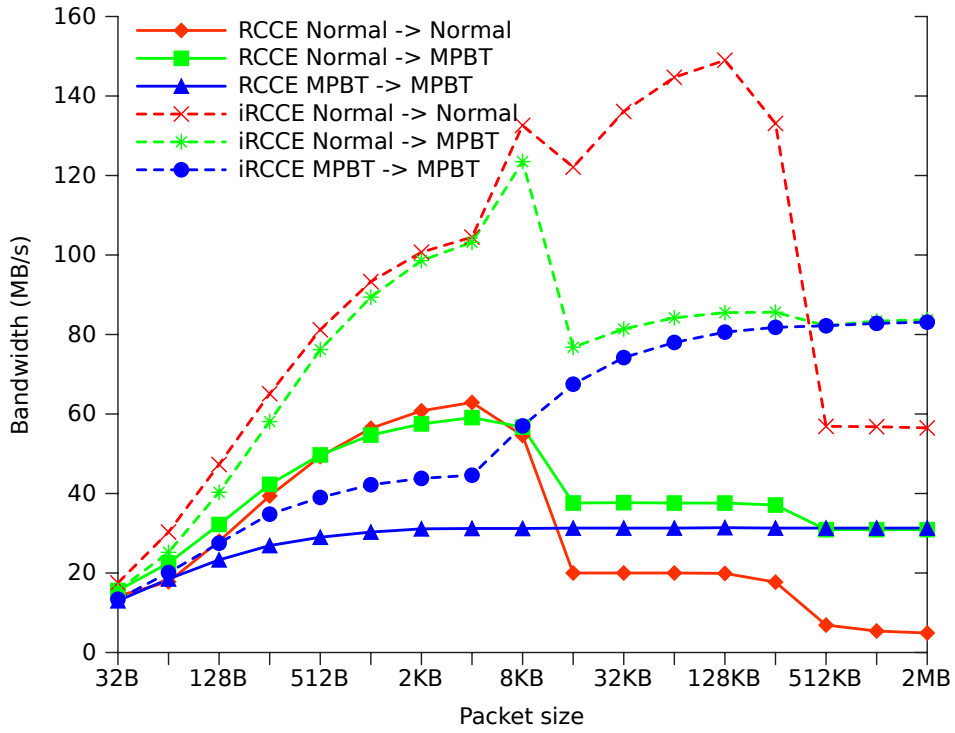

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- Cache flushing is expensive, but required to use cache-able shared memory.

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Power settings

- Voltage control
  - 6 *Voltage Islands* (4 tiles, 8 cores each)
  - Voltages from 0.6 to 1.3 Volt (stable from: 0.65625)
  - Adjustable at 0.0625 Volt steps (by hex value, $0.0625 = \frac{0.1}{16}$)

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- Frequency control
  - 24 *Frequency Islands* (1 tile, 2 cores each)
  - Frequency divider (2-16) from global 1600 MHz clock (800, 533, 400, ...)

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  - Only two voltage settings available 1.1, 0.8!
- Conclusion: We need to do it better and more easy!

Powerlib

- Working *Powerlib* after a bit of hacking and crashing the SCC (voltage too low for frequency)
- A better table (based on paper by P. Gschwandner):

Frequency divider	Frequency	Voltage
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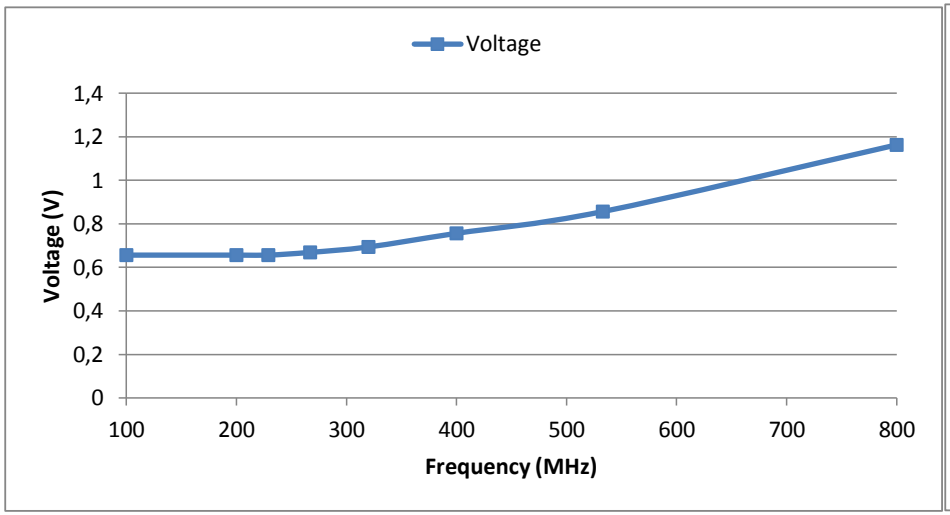
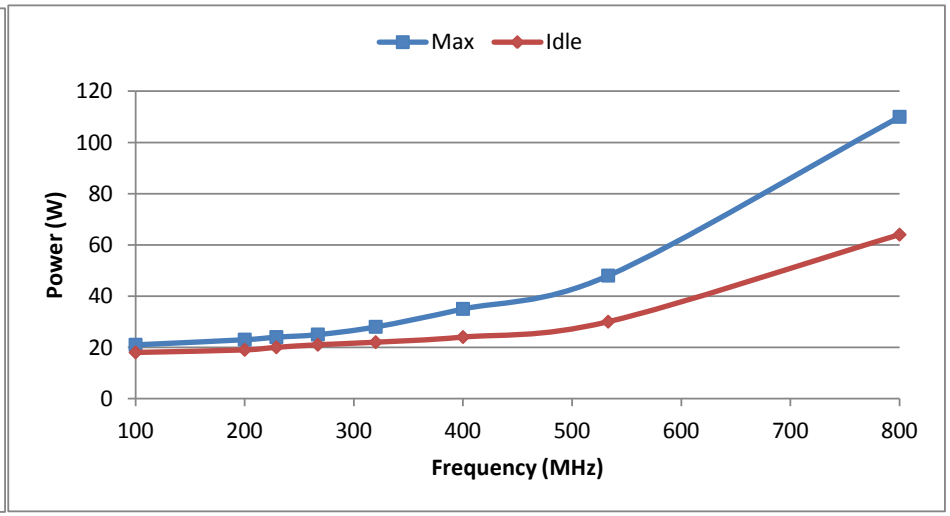
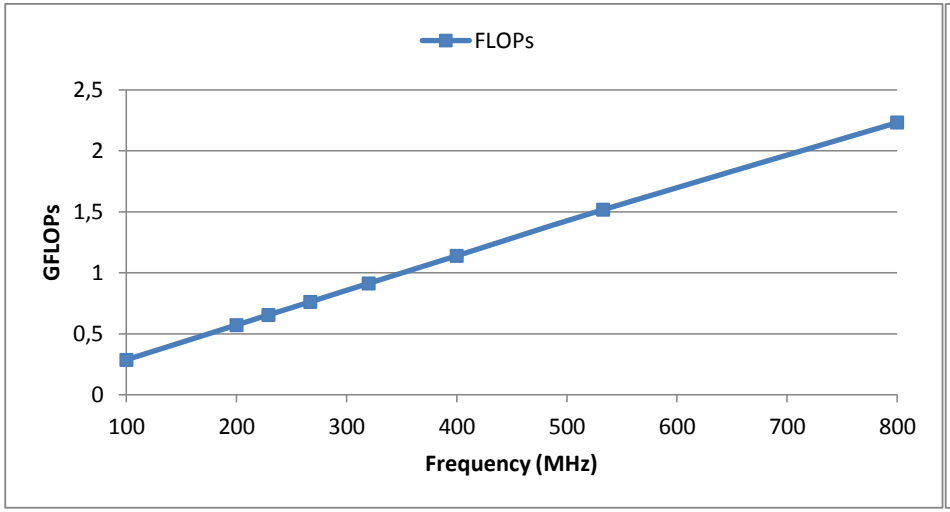
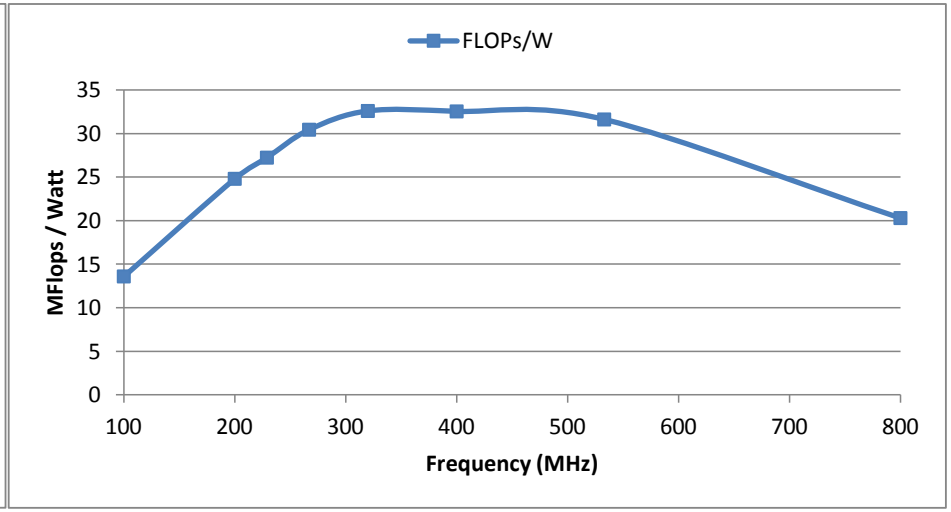
- Any core can set V/F values for chip
- Specify a domain and frequency, the library selects the highest possible frequency.
- Currently only control over Voltage Domains
  - Frequency scaling is not really effective when voltage is too high
  - Should support different frequencies for one Voltage Domain for fine-grained control

Energy Consumption









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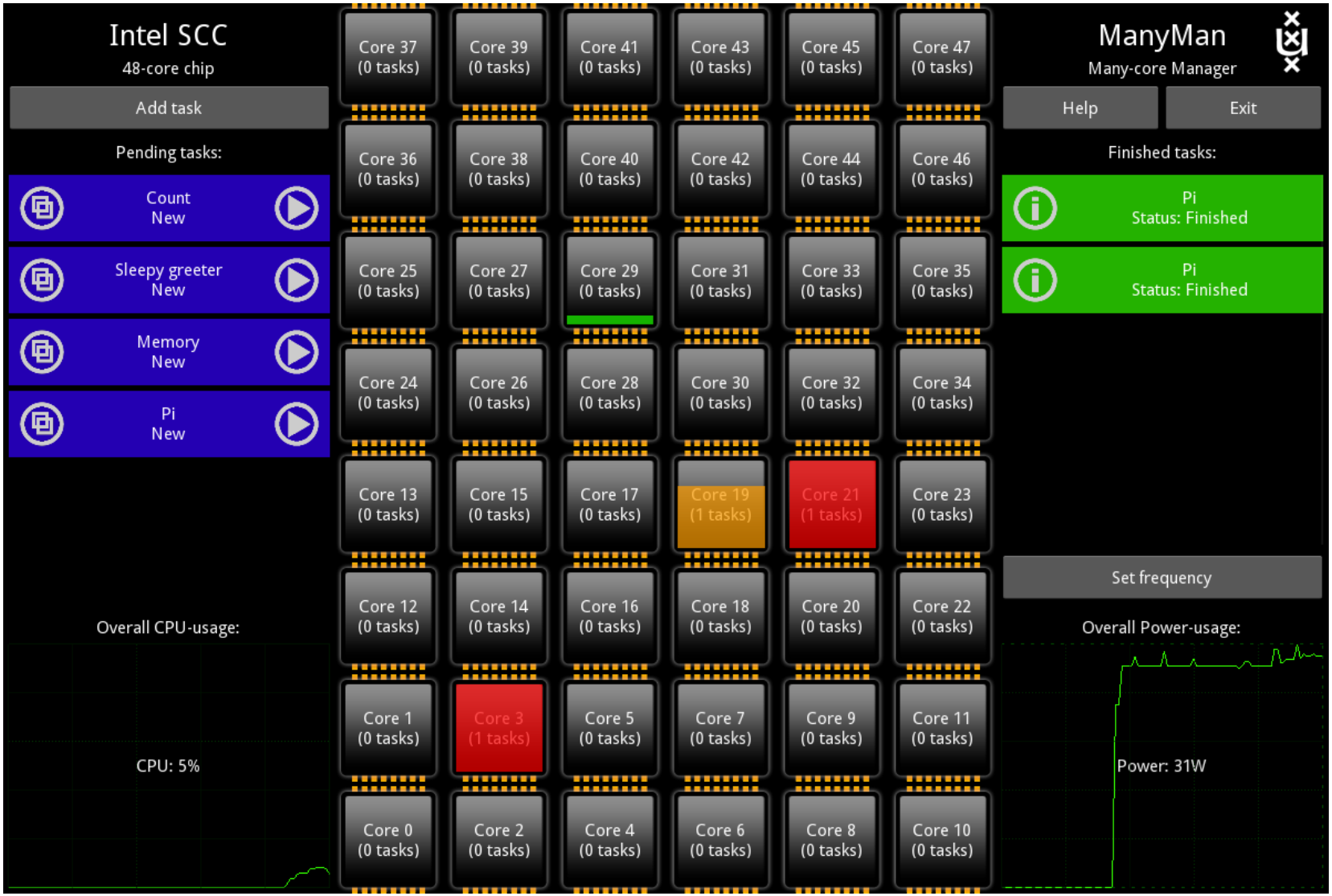
2. Manage the system:
   - Create a task
   - Start a task on a specified core
   - Migrate tasks
   - Modify frequency and voltage

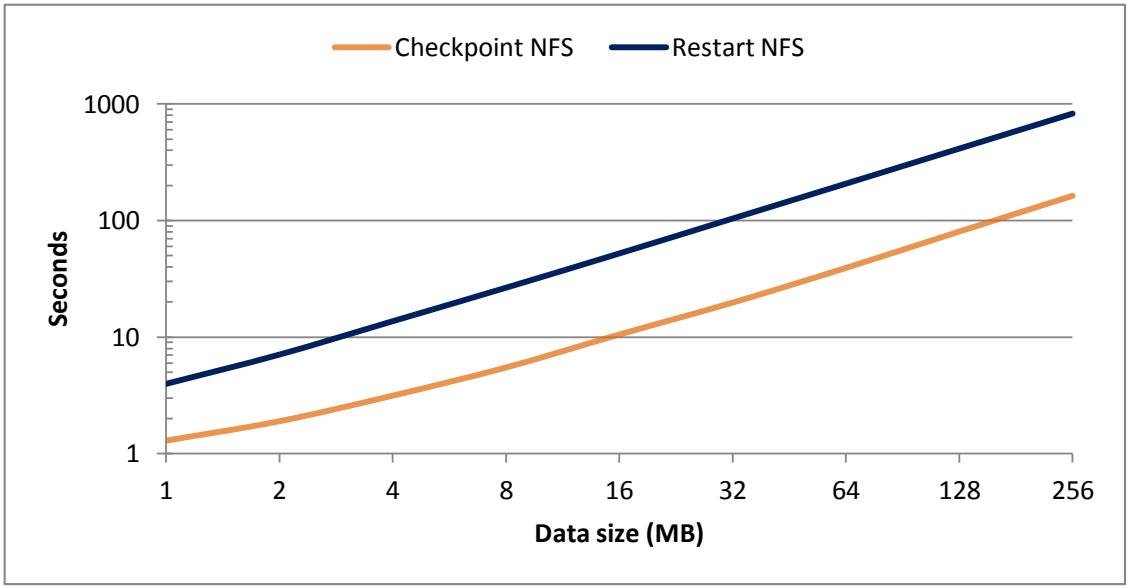
SCC Front-end

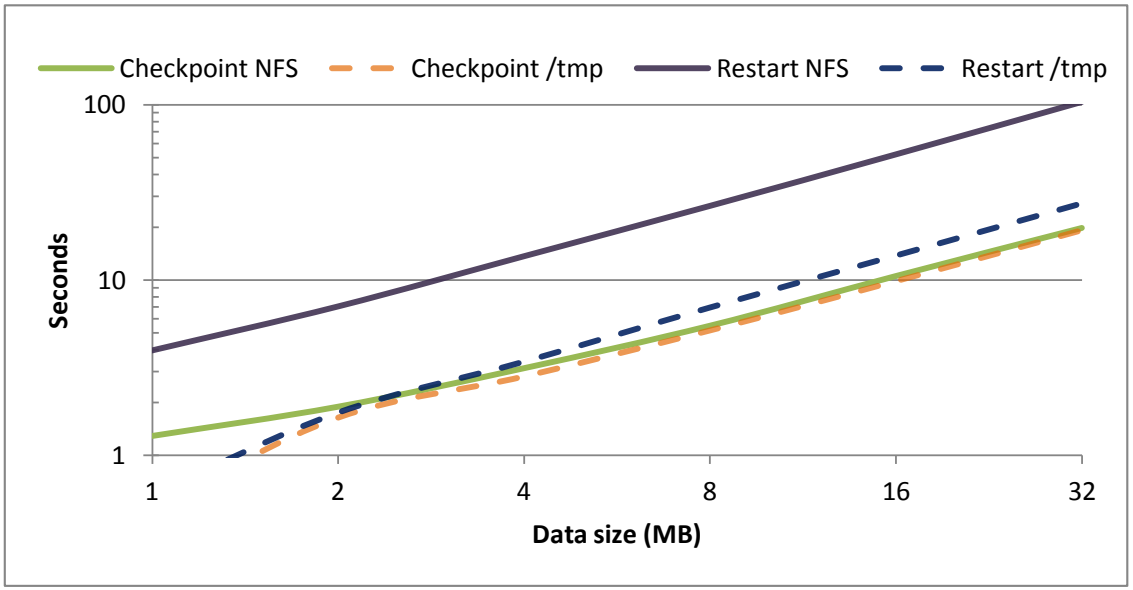


SCC Back-end

- Written in Python
- SSH for task creation on the SCC from MCPC
  - New `ssh` process for each task
  - SSH connection sharing improves latency
- Monitoring
  - `top`
  - `sccBmc`
- Managing
  - Berkeley Lab Checkpoint/Restart (BLCR)
  - The *Powerlib* is integrated in *ManyMan*

Migration using BLCR





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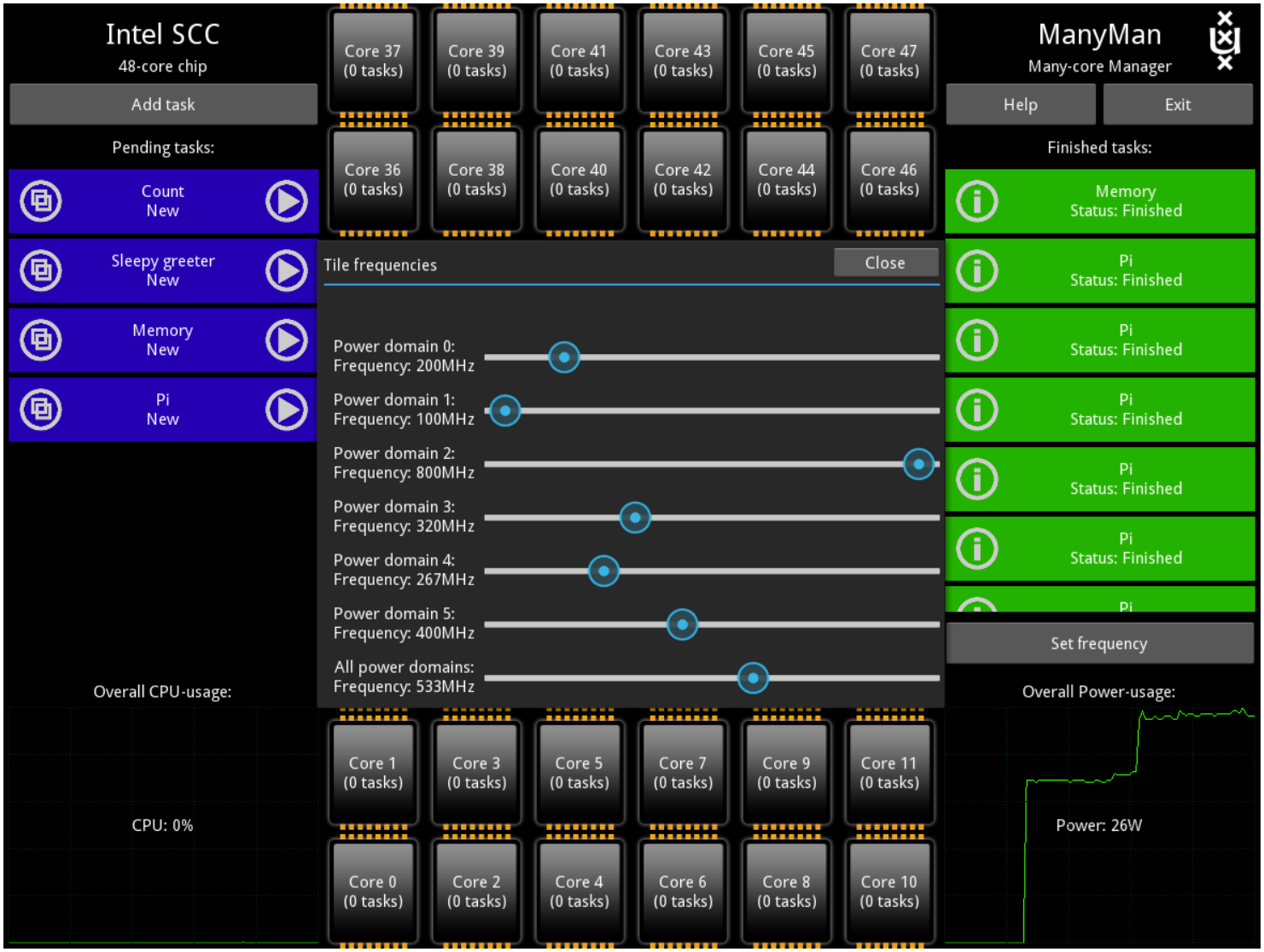

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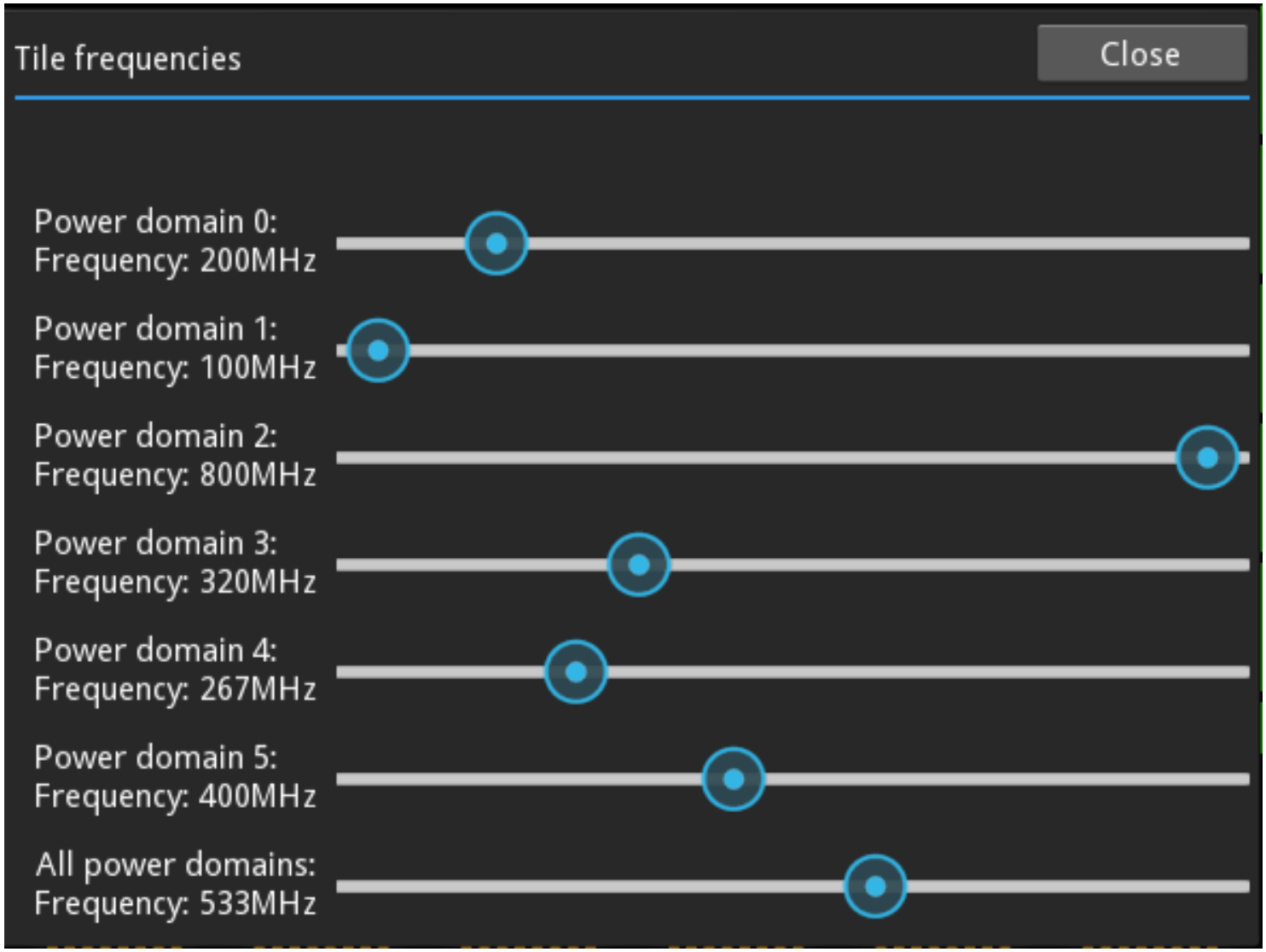

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Process Networks on the SCC

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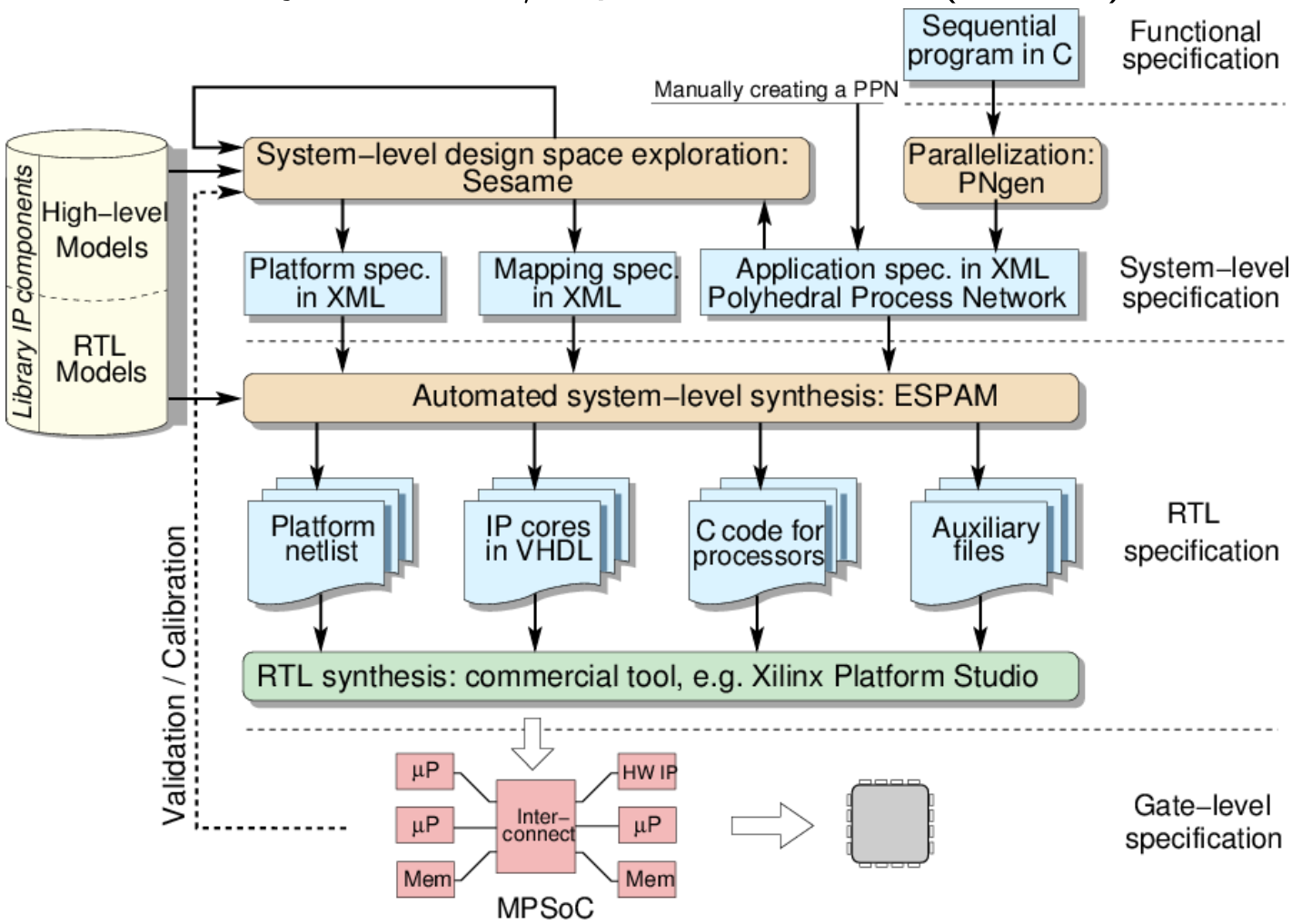

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- Need to modify channel implementation and code generation for SCC
- Should allow easy migration of light-weight processes (not like ManyMan...)
- Should allow for fine-grained V/F control

Outline

Reducing Overhead

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  - Encoding / Decoding with XDR to support heterogeneous platforms.
  - Implicit copy to a communication buffer.
- This can be avoided on the SCC:
  - No XDR: SCC cores are homogeneous.
  - Direct communication, data description function.
  - But this is only efficient for (large) arrays.

Implementation

- `mmap` two complete regions of 20 pages (20×16MB).
- Source region optimized for reading.
- Destination region optimized for writing (MPBT).
- Sending core requires L2 Flush.
- Receiving core maps MPBT+Write Through, so only `CL1INVMB` required.
- Beware of WCB issues.
- Bottleneck at cores that need to receive a lot at the same time.

Using Dedicated Copy Cores

- Dedicated copy cores run a *service* to copy memory regions.
- Communication protocol implemented using a ringbuffer in the MPB.
- L2 flush only on sending core, copycore use MPBT + WT.
- Communication is spread among all copy cores.
  - Threshold value for issuing copy cores
  - Split large copy operations over multiple copy cores.

Matrix Multiplication

- Split 2 input matrices to 2×4 sub matrices.
- Perform 8 matrix multiplications and 4 matrix additions on sub matrices (in parallel).
- Reconstruct new result matrix.
- Split can be performed recursive.

$$A \times B \rightarrow \begin{vmatrix} a1 & a2 \\ a3 & a4 \end{vmatrix} \times \begin{vmatrix} b1 & b2 \\ b3 & b4 \end{vmatrix} = \begin{vmatrix} a1 \times b1 & a1 \times b2 \\ a3 \times b1 & a3 \times b2 \end{vmatrix} + \begin{vmatrix} a2 \times b3 & a2 \times b4 \\ a4 \times b3 & a4 \times b4 \end{vmatrix} = \begin{vmatrix} c1 & c2 \\ c3 & c4 \end{vmatrix} \rightarrow C$$

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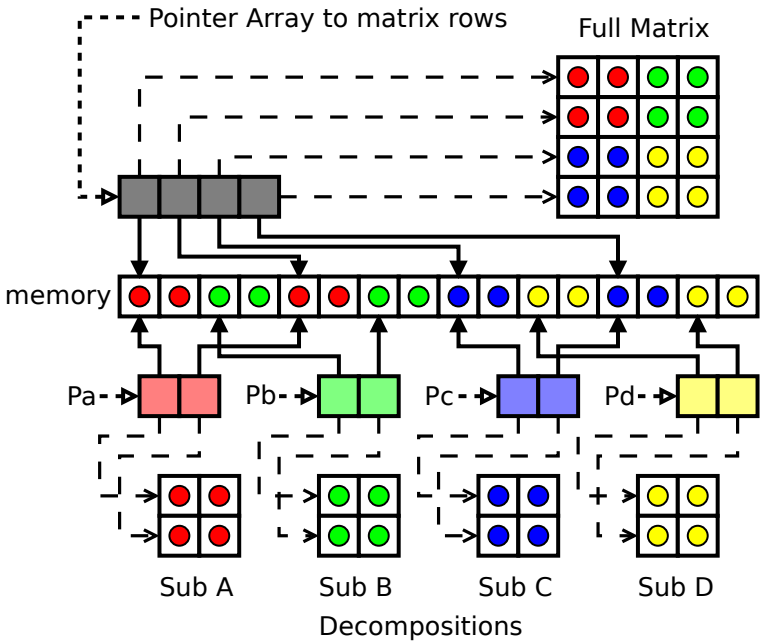

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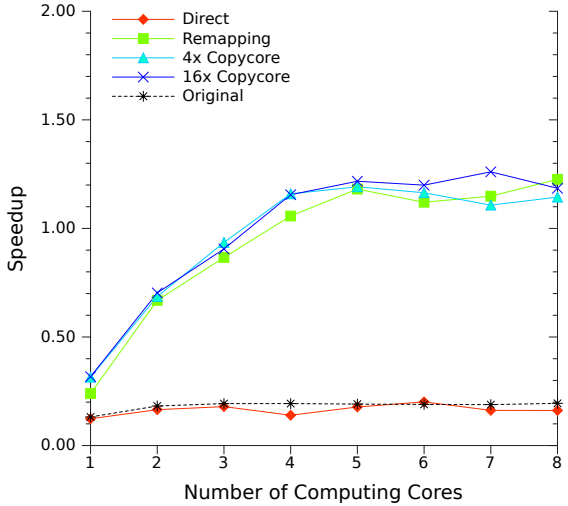
Matrix Multiplication - One recursion step

- Baseline: single thread on single core.



128×128

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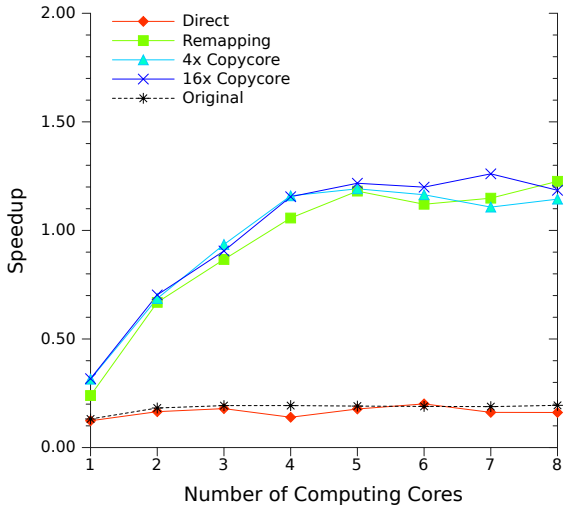
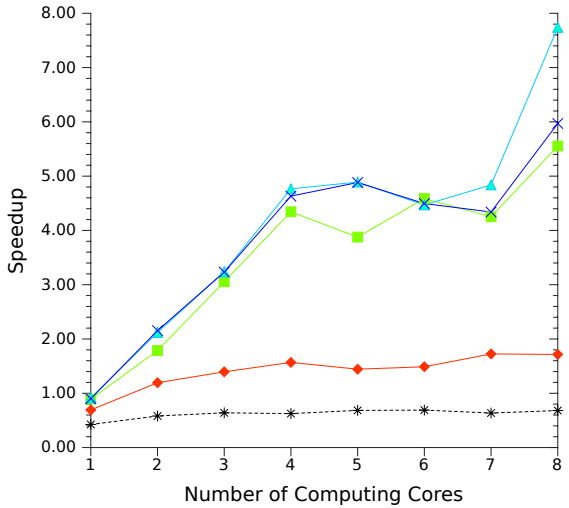


128×128



256×256

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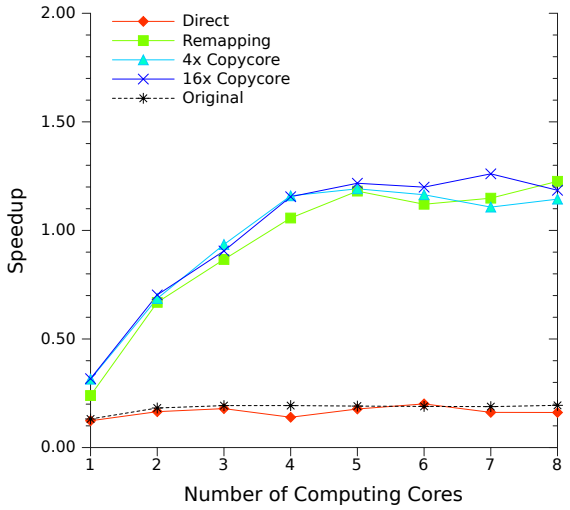
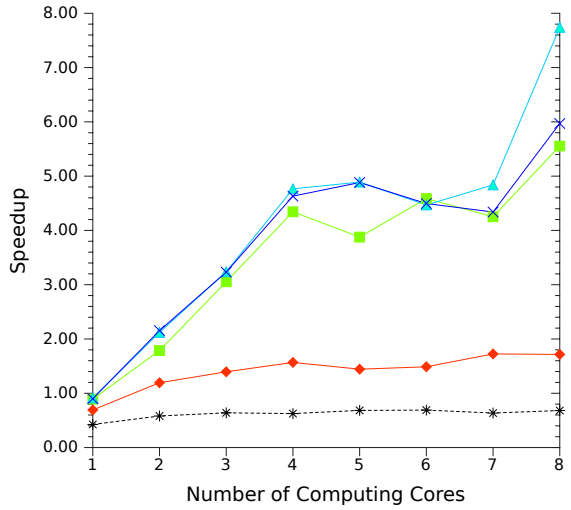
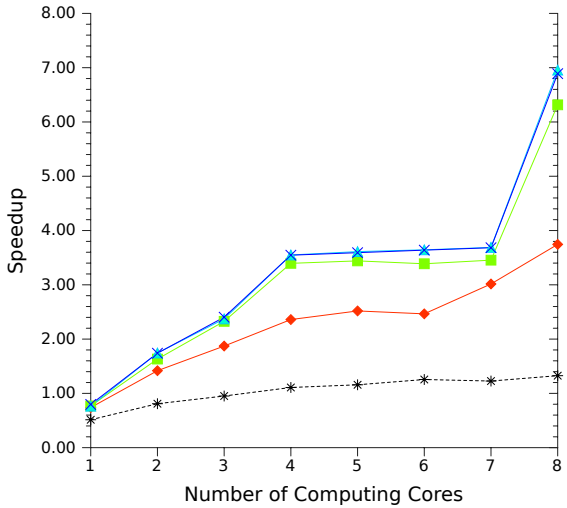


128 × 128



256 × 256



512 × 512

Matrix Multiplication - One recursion step

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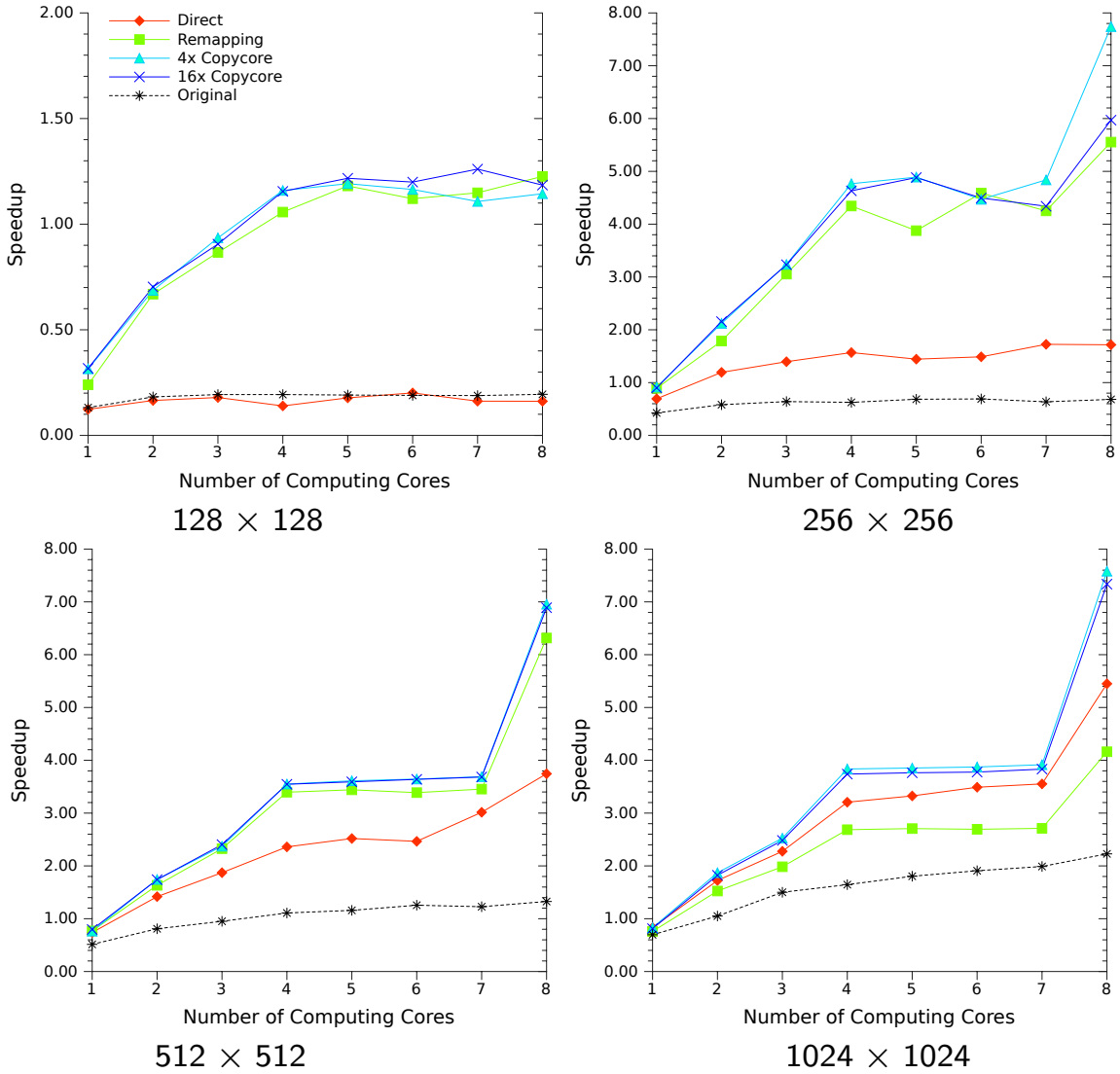
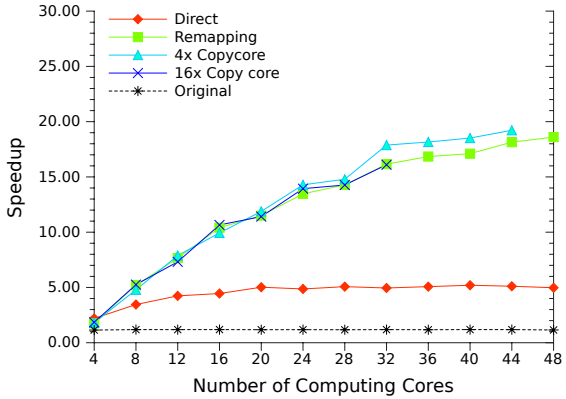


Matrix Multiplication - Two recursion steps

- Baseline: single thread on single core.



1024×1024

Matrix Multiplication - Two recursion steps

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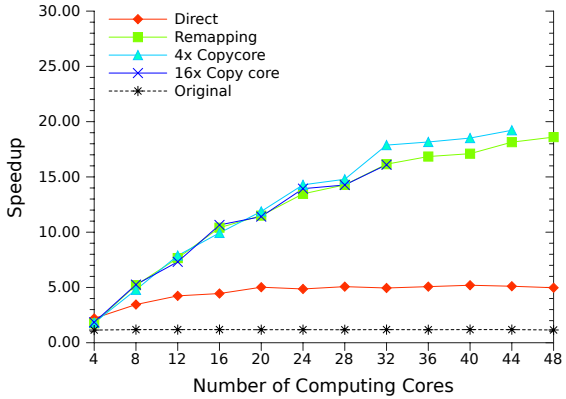

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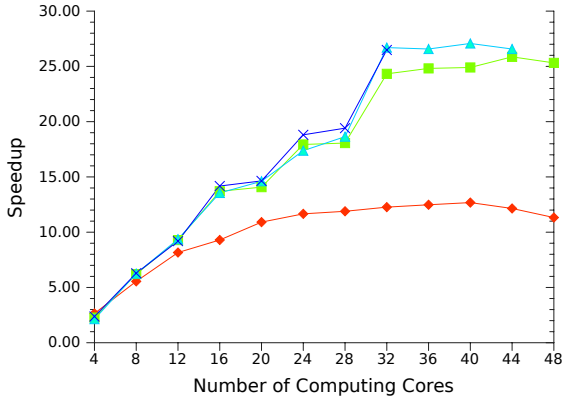

2048×2048

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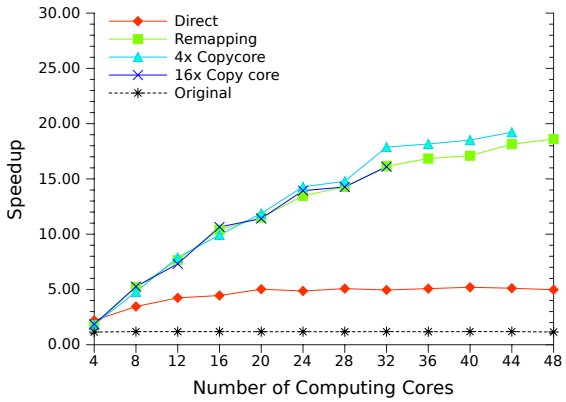

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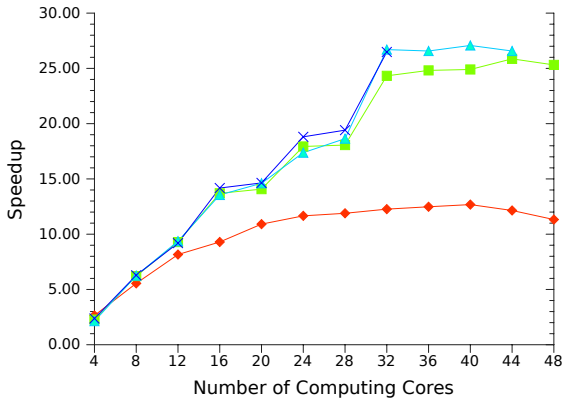
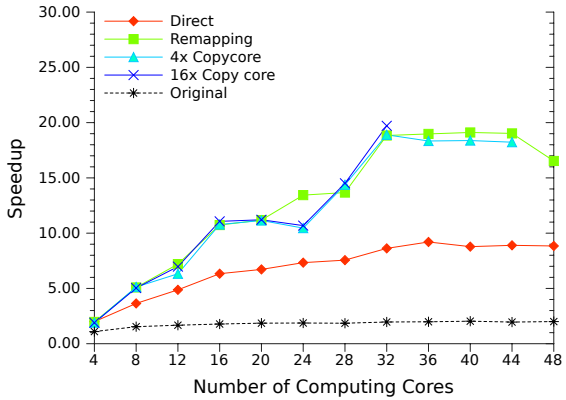


2048×2048



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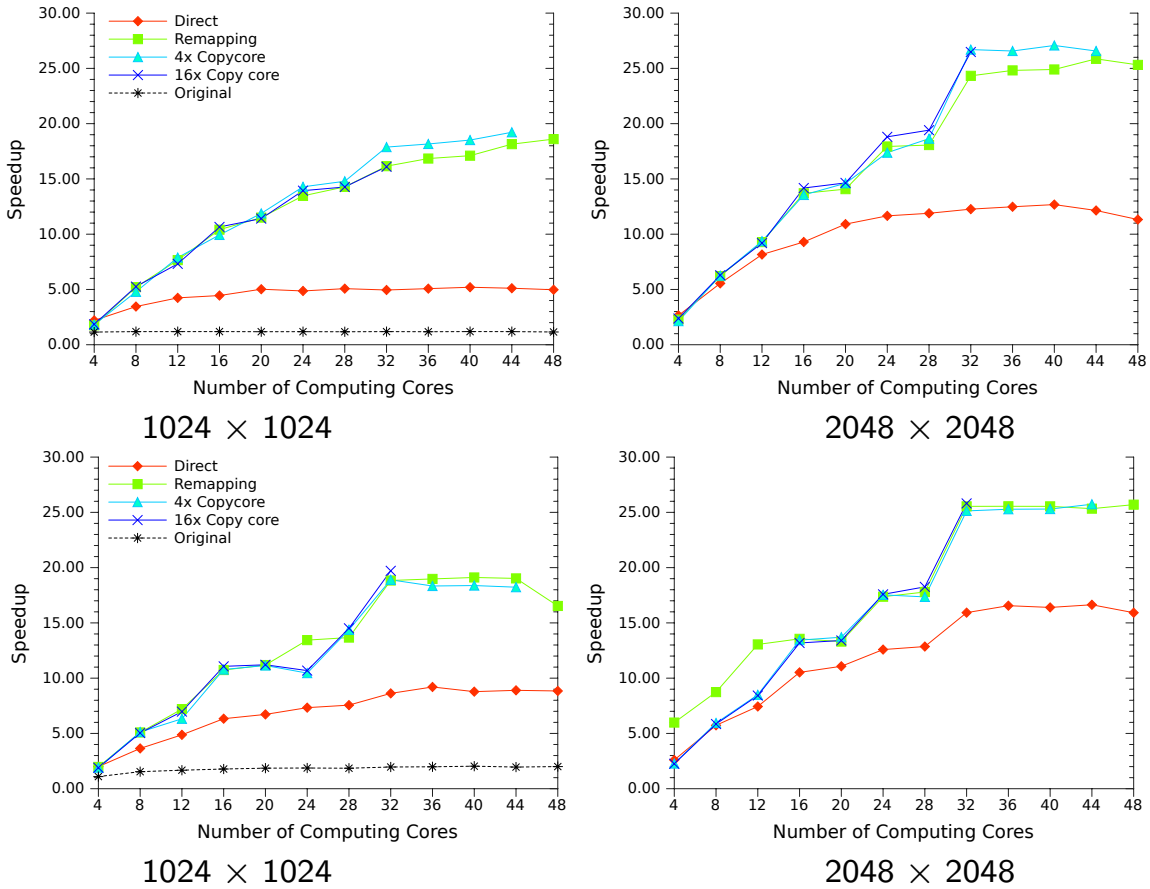

Questions

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Also feel free to ask off-line

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More info and references:

http://www.science.uva.nl/~bakkerr/