

nolimips

The MIPS Architecture Emulator
10 June 2014, NOLIMIPS Version 0.9a

Benoît Perrot

This manual is for Nolimips (version 0.9a, 10 June 2014), the tiny MIPS simulator.

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NOLIMIPS is a basic MIPS architecture simulator. It consists of an assembler which reads MIPS assembly code, and of a virtual machine which executes the instructions processed by the assembler. For the moment NOLIMIPS does not produce nor execute binary code, but ELF writer and loader are planned.

The main purpose of NOLIMIPS is to help students of compilers courses to evaluate the output from their "high-level language into MIPS assembler code" compilers, before and after register allocation.

Its features are:

- minimal support of MIPS instruction set
- built-in system calls (string printing and reading, etc.)
- unlimited registers (\$x0, \$x1, etc.).

It was written by Benoît Perrot as an LRDE member, so that EPITA students could exercise their compiler projects after the instruction selection but before the register allocation. It is implemented in C++ and Python. Be aware that NOLIMIPS does not need a Python interpreter to run, it is only required to maintain NOLIMIPS.

Information about NOLIMIPS can be found on the NOLIMIPS Home Page¹, and feedback can be sent to lrde's Projects Address². LRDE stands for Laboratoire de Recherche et Développement de l'EPITA³, i.e., the Research and Development Lab of EPITA, the Ecole Pour l'Informatique et les Techniques Avancées⁴.

Andrew Appel's home page⁵ includes links to material related to compilers theory, and some information about the Modern Compiler Implementation⁶ book series.

More information on Python can be found on Python Home Page⁷.

¹ NOLIMIPS Home Page, <https://www.lrde.epita.fr/wiki/Nolimips>.

² lrde's Projects Address, projects@lrde.epita.fr.

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⁵ Andrew Appel's home page, <http://www.cs.princeton.edu/~appel/>.

⁶ Modern Compiler Implementation, <http://www.cs.princeton.edu/~appel/modern/>.

⁷ Python Home Page, <http://www.python.org>.

1 Invoking Nolimips

To invoke `nolimips` run:

```
nolimips options file
```

where ‘`file.s`’ is a simple text file, and *options* is any combination of the following options:

‘`-h`’

‘`--help`’ Display a help message and exit successfully.

‘`-V`’

‘`--version`’

Display the version number and exit successfully.

‘`--usage`’ Give a short usage message

‘`--tasks-selection`’

Each task of NOLIMIPS (parsing, execution, etc.) comes with a set of prerequisites: for example the pretty printing of an input program implies the parsing of its source file. This option asks NOLIMIPS to display the tasks that must be run before to run the ones explicitly specified on command line.

‘`--parse`’ Parse a file.

‘`--trace-scan`’

Trace the scanning.

‘`--trace-parse`’

Trace the parse.

‘`-N`’

‘`--nop-after-branch`’

To avoid a bubble in their pipeline, MIPS processors execute the instruction immediately following a branch; this instruction is said to be in the delay slot (FIXME: see further). This option fills the delay slot of branch instructions with a NOP, disabling the delay slot, simplifying the task of assembly programmers how do not care about writing optimized code.

‘`-u`’

‘`--unlimited-regs`’

During last stages of a compiler, the intermediate representation of a source file (which mainly consists in a generic, architecture independent assembly code) is progressively translated into an architecture dependent assembly code. Low level (but still intermediate) representations are designed to be as near as possible of target assembly code, but generally consider an extended target machine with an unlimited amount of registers. This option gives NOLIMIPS the ability to handle an arbitrary number of registers, allowing compiler developpers to test their low level output before implementing register allocation. These new registers may be used as any other MIPS registers through the symbols `$x0`, `$x1`, and so on. They have a general purpose and are not considered as caller save nor callee save registers.

‘`--prg-display`’

Display the read program.

`--prg-solve` Resolve jump offsets and check bounds of immediates.

`--callee-save=num`
`--caller-save=num`
`--argument-registers=num` Respectively set the maximum number of callee-save, caller-save and argument registers to *num*, a positive number.

`--check-callee-save` Warn if a callee save register is not preserved across a call.

`--profile` Enable program profiling

`-l library`
`--system-library=library` Specify the builtin system library to use. Accepted *library* values are `spim` (selected by default and implementing SPIM's¹ behavior), `nolimips` (NOLIMIPS' own library), and `none` (no builtin library).

`-e`
`--execute` Execute the program on virtual machine.

`-E`
`--trace-exec` Trace the execution.

`-i`
`--shell` Launch interactive shell.

¹ SPIM's, <http://spimsimulator.sourceforge.net/>.

2 Internal of Nolimips

2.1 Steps of Nolimips

NOLIMIPS works in three steps:

- it scans and parses the file (lexical and syntactical analysis), producing an abstract representation of a program;
- it resolves the program, checking the existence of labels used and computing branch offsets (assembly);
- it loads the resolved program in the virtual machine, search for an entry point labeled `main` and start execution (execution).

3 The Nolimips Language

NOLIMIPS supports a minimal MIPS instruction set and unlimited registers.

3.1 The Nolimips supported instruction set

3.1.1 Arithmetic instructions

3.1.1.1 ADD

Add src1 and src2 and store the result in dest (32-bit integers). If an overflow occurs, then trap.

3.1.1.2 ADDU

Add src1 and src2 and store the result in dest (32-bit integers).

3.1.1.3 ADDI

Add a constant imm and src and store the result in dest (32-bit integers). If overflow occurs, then trap.

3.1.1.4 ADDIU

Add a constant imm and src and store the result in dest (32-bit integer).

3.1.1.5 SUB

Subtract src2 from src1 and store the result in dest (32-bit integers). If an overflow occurs (FIXME), then trap.

3.1.1.6 SUBU

Subtract src2 from src1 and store the result in dest (32-bit integers).

3.1.1.7 NEG

Negate (logical 2-complement) src and store the result in dest. If an overflow occurs (FIXME), then trap.

3.1.1.8 NEGU

Negate src (logical 2-complement) and store the result in dest.

3.1.1.9 ABS

Compute the absolute value of src (32-bit integer) and write it to dest.

3.1.1.10 MUL

Multiply two words src1 and src2 and write the result to dest.

3.1.1.11 DIV

Divide src1 by src2 (32-bit signed integers), write the quotient in LO and the remainder in HI (32-bit integer).

3.1.1.12 DIVU

Divide src1 by src2 (32-bit unsigned integers), write the quotient in LO and the remainder in HI (32-bit integer).

3.1.1.13 REM

Compute the remainder from dividing src1 by src2 (32-bit signed integers) and write it to dest.

3.1.1.14 REMU

Compute the remainder from dividing src1 by src2 (32-bit unsigned integers) and write it to dest.

3.1.2 Bitwise instructions

3.1.2.1 SLL

Left-shift (logical) the word src by the fixed number imm of bits and store the result in dest.

3.1.2.2 SLLV

Left-shift (logical) the word src1 by the variable number src2 of bits and store the result in dest.

3.1.2.3 SRA

Right-shift (arithmetic) the word src by the fixed number imm of bits and store the result in dest.

3.1.2.4 SRAV

Right-shift (arithmetic) the word src1 by the variable number src2 of bits and store the result in dest.

3.1.2.5 SRL

Right-shift (logical) the word src1 by the variable number src2 of bits and store the result in dest.

3.1.2.6 SRLV

Right-shift (logical) the word src1 by the variable number src2 of bits and store the result in dest.

3.1.2.7 ROL

Left-rotate the word `src` by a number of bits (`imm` or `src2`) and store the result in `dest`.

3.1.2.8 ROR

Right-rotate the word `src` by a number (`imm` or `src2`) of bits and store the result in `dest`.

3.1.2.9 AND

Compute the bitwise logical AND between `src1` and `src2` and store the result to `dest`.

3.1.2.10 ANDI

Compute the bitwise logical AND between `src` and a constant `imm` and store the result to `dest`.

3.1.2.11 OR

Compute the bitwise logical OR between `src1` and `src2` and store the result to `dest`.

3.1.2.12 ORI

Compute the bitwise logical OR between `src` and a constant `imm` and store the result to `dest`.

3.1.2.13 XOR

Compute the bitwise logical XOR between `src1` and `src2` and store the result to `dest`.

3.1.2.14 XORI

Compute the bitwise logical XOR between `src` and a constant `imm` and store the result to `dest`.

3.1.2.15 NOR

Compute the bitwise logical NOR between `src1` and `src2` and store the result to `dest`.

3.1.2.16 NOT

Negate (logical 1-complement) `src` and store the result in `dest`.

3.1.3 Comparison instructions

3.1.3.1 SEQ

Set `dest` to 1 if `src1` equals `src2`, else clear it.

3.1.3.2 SNE

Set `dest` to 1 if `src1` does not equal `src2`, else clear it.

3.1.3.3 SGE

Set `dest` to 1 if `src1` is greater or equal to `src2` (signed comparison), else clear it.

3.1.3.4 SGEU

Set dest to 1 if src1 is greater or equal to src2 (unsigned comparison), else clear it.

3.1.3.5 SGT

Set dest to 1 if src1 is greater than src2 (signed comparison), else clear it.

3.1.3.6 SGTU

Set dest to 1 if src1 is greater than src2 (unsigned comparison), else clear it.

3.1.3.7 SLE

Set dest to 1 if src1 is lower or equal to src2 (signed comparison), else clear it.

3.1.3.8 SLEU

Set dest to 1 if src1 is lower or equal to src2 (unsigned comparison), else clear it.

3.1.3.9 SLT

Set dest to 1 if src1 is lower than src2 (signed comparison), else clear it.

3.1.3.10 SLTU

Set dest to 1 if src1 is lower than src2 (unsigned comparison), else clear it.

3.1.3.11 SLTI

Set dest to 1 if src1 is lower than a constant imm (signed comparison), else clear it.

3.1.3.12 SLTIU

Set dest to 1 if src1 is lower than a constant imm (unsigned comparison), else clear it.

3.1.4 Branch instructions**3.1.4.1 BEQ**

Branch to label if src1 equals src2.

3.1.4.2 BEQZ

Branch to label if src equals zero.

3.1.4.3 BNE

Branch to label if src1 does not equal src2.

3.1.4.4 BNEZ

Branch to label if src does not equal zero.

3.1.4.5 BGE

Branch to label if src1 is greater or equal to src2 (signed comparison).

3.1.4.6 BGEU

Branch to label if src1 is greater or equal to src2 (unsigned comparison).

3.1.4.7 BGEZ

Branch to label if src is greater or equal to zero (signed comparison).

3.1.4.8 BGEZAL

Call label if src is greater or equal to zero (signed comparison)

3.1.4.9 BGT

Branch to label if src1 is greater than src2 (signed comparison).

3.1.4.10 BGTU

Branch to label if src1 is greater than src2 (unsigned comparison).

3.1.4.11 BGTZ

Branch to label if src is greater than zero (signed comparison).

3.1.4.12 BLE

Branch to label if src1 is lower or equal to src2 (signed comparison).

3.1.4.13 BLEU

Branch to label if src1 is lower or equal to src2 (unsigned comparison).

3.1.4.14 BLEZ

Branch to label if src is lower or equal to zero (signed comparison).

3.1.4.15 BLT

Branch to label if src1 is lower than src2 (signed comparison).

3.1.4.16 BLTU

Branch to label if src1 is lower than src2 (unsigned comparison).

3.1.4.17 BLTZ

Branch to label if src1 is lower than zero (signed comparison).

3.1.4.18 BLTZAL

Call label if src1 is lower than zero (signed comparison).

3.1.4.19 J

Jump to label unconditionally.

3.1.4.20 JAL

Call label unconditionally.

3.1.4.21 JR

Jump to address contained in dest unconditionally.

3.1.4.22 JALR

Call address contained in dest unconditionally.

3.1.5 Load instructions

3.1.5.1 LB

Load the 8-bit quantity at address (offset + base) into dest as a signed value.

3.1.5.2 LBU

Load the 8-bit quantity at address (offset + base) into dest as an unsigned value.

3.1.5.3 LW

Load the 32-bit quantity at address (offset + base) into dest as a signed value.

3.1.5.4 LUI

Move the constant imm into the upper half word of dest.

3.1.5.5 LI

Move the constant imm into dest.

3.1.5.6 LA

Move the computed address into dest.

3.1.6 Store instructions

3.1.6.1 SB

Store the low byte from src at address (offset + base).

3.1.6.2 SW

Store the low word from src at address (offset + base).

3.1.7 Movement instructions

3.1.7.1 MOVE

Move the contents of src to dest.

3.1.7.2 MFHI

Move the contents of HI to dest.

3.1.7.3 MFLO

Move the contents of LO to dest.

3.1.7.4 MTHI

Move the contents of dest to HI.

3.1.7.5 MTLO

Move the contents of dest to LO.

3.1.7.6 MFC0

Move the contents of control coprocessor src register to CPU dest register.

3.1.7.7 MTC0

Move the contents of CPU src register to control coprocessor dest register.

3.1.8 Syscall instructions

3.1.8.1 SYSCALL

Raise a system call exception.

3.1.9 Nop instructions

3.1.9.1 NOP

To do nothing.

3.2 Nolimips features

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